REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-2, 18-19 and 22-31 are presently active in this case, Claims 3-15 have been canceled without prejudice, Claims 16-17 and 20-21 are canceled without prejudice by the present amendment, Claims 1 and 18-19 are amended, and Claims 24-31 are added by the present amendment. No new matter is added.

In the outstanding Official Action, Claims 1, 2, 22 and 23 were rejected under 35 U.S.C. 103(a) as obvious of Gerber et al. (U.S. Patent No. 5,401,913) in view of either one of Bohn (U.S. Patent No. 6,537,412) or Johnston (U.S. Patent No. 5,153,050) and Daigle et al. (U.S. Patent No. 5,046,238). Claims 16, 17, 22 and 23 were rejected under 35 U.S.C. 103(a) as obvious of Gerber et al., either one of Bohn or Johnston and Daigle et al. and further in view of Enomoto et al. (WO 98/56220). Claims 18-21 were rejected under 35 U.S.C. 103(a) as obvious of Gerber et al., either one of Bohn or Johnston and Daigle et al. and further in view of Kimura et al. (U.S. Patent No. 6,376,782).

Regarding the rejection under 35 U.S.C. 103(a), Applicants respectfully traverse the outstanding grounds for rejection, because in Applicants' view, independent Claim 1 patentably distinguishes over the applied references as discussed below.

Claim 1 recites, *inter alia*, "***stacking an outermost copper foil on the bonding layer*** of the printed board with the conductor circuit" and "integrating the second printed board, the printed board with the conductor circuit, and the outermost copper foil by ***heating and one time of pressing*** such that ***the conductive bump*** in each printed board ***pierces through the corresponding bonding layer*** covering the conductive bump ***and is electrically connected to*** corresponding one of the conductor circuit and ***the outermost copper foil.***"

The outstanding Office Action acknowledges that Gerber et al. does not teach an upper outermost copper conductor layer (Office Action at page 3, lines 12-13). Instead, the

outstanding Office Action states that Gerber et al. teaches the multilayer circuit board of Fig. 9 is connected on its upper side to substrates including a copper conductor layer to form an integral, operable multilayer circuit board (Office Action at page 3, lines 13-16). Further, the outstanding Office Action relies on Bohn and Johnston to remedy the deficiencies of Gerber et al., indicating that Bohn and Johnston both disclose placing outermost copper foils covering the entire surface of the outermost printed circuit boards on the stack (Office Action at page 3, line 6 though page 4, line 3).

First, the fact that Gerber et al. describes the device as being electrically connected in some manner does not inherently teach "stacking an outermost copper foil on the bonding layer of the printed board with the conductor circuit," as recited in Claim 1. There are alternatives, such as a wire bonding and a solder, to electrically connect the device to another circuit. Thus, Gerber et al. fails to teach or suggest that an outermost copper foil is stacked on the bonding layer and that the conductive bump pierces through the bonding layer and is electrically connected to the outermost copper foil.

Second, Bohn shows in Fig. 1 a multilayer (1) comprising inner layers (3), intermediate layers (4) and outer foils (2a, 2b). The intermediate layers (4) are impregnated with adhesives, the so-called prepregs (Bohn at col. 1, lines 53-55). The inner layers (3) are connected to the outer foils (2a, 2b) with the intermediate layers (4) formed therebetween as adhesives. However, Bohn does not teach or suggest that the strip conductors (3a) pierce through the intermediate layers (4) and are electrically connected to the outer foils (2a, 2b). Even if the outer foils (2a, 2b) constitute layers of the multilayer (1) and are electrically connected to the strip conductors (3a), Bohn does not teach or suggest that the strip conductors (3a) pierce through the intermediate layers (4). Thus, Bohn fails to teach or suggest that an outermost copper foil is stacked on the bonding layer and that the conductive

bump pierces through the bonding layer and is electrically connected to the outermost copper foil.

Third, Johnston shows in Fig. 1 a multilayer comprising a core (10) and copper foil layers (4). The core includes prepreg layers (12) and boards (14) with conductive paths (15) formed thereon. The upper surface (8) and the lower surface (16) of the foil layers (4) may be oxidized to facilitate better bonding with prepreg layers (12) (Johnston at col. 4, lines 34-36 and 41-44). The boards (14) are connected to the foil layers (4) with the prepreg layers (12) formed therebetween as adhesives. However, Johnston does not teach or suggest that the conductive paths (15) pierce through the prepreg layers (12) and are electrically connected to the foil layers (4). Even if the foil layers (4) are electrically connected to the conductive paths (15), Johnston does not teach or suggest that the conductive paths (15) pierce through the prepreg layers (12). Thus, Johnston fails to teach or suggest that an outermost copper foil is stacked on the bonding layer and that the conductive bump pierces through the bonding layer and is electrically connected to the outermost copper foil.

Accordingly, even the combination of Gerber et al., Bohn and Johnston does not teach or suggest "***stacking an outermost copper foil on the bonding layer*** of the printed board with the conductor circuit" and "integrating the second printed board, the printed board with the conductor circuit, and the outermost copper foil by heating and one time of pressing such that ***the conductive bump*** in each printed board ***pierces through the corresponding bonding layer*** covering the conductive bump ***and is electrically connected to*** corresponding one of the conductor circuit and ***the outermost copper foil***," as recited in Claim 1.

Thus, independent Claim 1 patentably distinguishes over the applied references. Therefore, Claim 1 and the pending Claims 2 and 18-25 dependent from Claim 1 are believed to be allowable.

It is noted that the applied references do not teach or suggest "integrating the stacked printed boards and the outermost copper foil by heating and pressing the copper foil of the first printed board and the outermost copper foil such that the conductive bumps of the plurality of the printed boards pierce through the corresponding bonding layers covering the conductive bumps and are electrically connected to the copper foils facing the respective bonding layers, and the conductive bump of the second printed board pierces through the corresponding bonding layer covering the conductive bump and is electrically connected to the outermost copper foil," as recited in new independent Claim 26.

Thus, new independent Claim 26 and the pending Claims 27-31 dependent from Claim 26 are believed to be allowable.

In view of the amendments and discussions presented above, Applicant respectfully submits that the present application is in condition for allowance, and an early action favorable to that effect is earnestly solicited.

Respectfully submitted,

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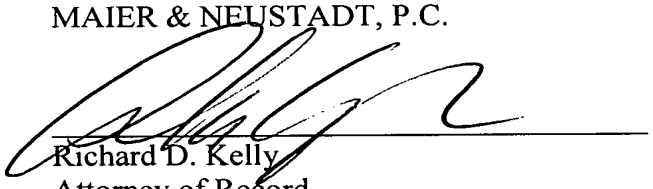

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